Amendments to the Claims

The following listing of claims shall supercede all previously submitted versions.

Claims Listing

1-28 (Cancelled).

29. (Currently Amended) An electrostatic discharge circuit for connecting between a first power supply voltage source and a second power supply voltage source to protect internal integrated circuits from damage due to an electrostatic discharge, said electrostatic discharge circuit comprising:

first and second power supply voltage sources;

an internal integrated circuit located between the first and second power supply voltage sources;

a substrate;

a plurality of serially connected polycrystalline silicon diodes formed on the substrate, each diode having a first portion that is heavily doped with an impurity of a first type and a second portion that is heavily doped with an impurity of a second type, the first and second portions being adjoined to form an electrical junction;

wherein the second portion of one of the plurality of diodes is connected to the first portion of a subsequent one of the plurality of diodes; ~~and~~

wherein a first diode of the plurality of diodes has its first portion connected to the first power supply voltage source, and a last diode of the plurality of diodes has its second portion connected to the second power supply voltage source; and

wherein the plurality of serially connected polycrystalline silicon diodes comprises "n" diodes, and the number "n" is determined by the formula:

$n >= (V_{noise} + |Vx1 - Vx2|) / V_T$

where:

n is the number of serially connected polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuit located between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,
Vx2 is the magnitude of the second power supply voltage source, and
V_T is the threshold voltage of each of the polycrystalline silicon diodes.

30. (Previously Presented) The electrostatic discharge circuit of claim 29, wherein the first and second portions of each diode are formed on a region of shallow trench isolation that is formed within the substrate.

31. (Previously Presented) The electrostatic discharge circuit of claim 30, wherein an insulating layer is disposed between each region of shallow trench isolation and the substrate.

32. (Previously Presented) The electrostatic discharge circuit of claim 29, wherein each diode further comprises an oxide layer that overlays at least part of the first and second portions at the connection therebetween.

33. (Previously Presented) The electrostatic discharge circuit of claim 29, wherein the first portion of each diode is a cathode and the second portion of each diode is an anode.

34. (Previously Presented) The electrostatic discharge circuit of claim 33, wherein the impurity of the first type is an N-type impurity having a density of from approximately 10^{15} atoms/cm^3 to approximately 10^{21} atoms/cm^3.

35. (Previously Presented) The electrostatic discharge circuit of claim 33, wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^3 to approximately 10^{21} atoms/cm^3.

36. (Previously Presented) The electrostatic discharge circuit of claim 33, wherein each of the diodes has a thickness of from approximately 1000Å to approximately 3000Å.

37. (Previously Presented) The electrostatic discharge circuit of claim 33, wherein each of the diodes has a thickness of from approximately 0.5 μm to approximately 100 μm.

38. (Cancelled)

39. (Currently Amended) An integrated circuit formed on a substrate comprising:

first and second power supply voltage sources;

an internal integrated circuit located between the first and second power supply voltage sources;

a first power distribution network connected to the first power supply voltage source;

a second power distribution network connected to the second power supply voltage source;

an internal circuit connected between the first and second power distribution networks; and

an electrostatic discharge circuit connected between the first power supply voltage source and the second power supply voltage source to protect the internal circuit from a electrostatic discharge (ESD), said electrostatic discharge circuit comprising:

a substrate;

a plurality of serially connected polycrystalline silicon diodes formed on the substrate, each diode having first electrode comprising a first region of polycrystalline silicon heavily doped with an impurity of a first type and a second electrode comprising a second region of polycrystalline silicon heavily doped with an impurity of a second type, said first and second regions being connected to form an electrical junction;

wherein the second portion of one of the plurality of diodes is connected to the first portion of a subsequent one of the plurality of diodes; ~~and~~

wherein a first diode of the plurality of diodes is connected to the first power supply voltage source and a last diode of the plurality of diodes is connected to the second power supply voltage source; and

wherein the plurality of serially connected polycrystalline silicon diodes comprises "n" diodes, and the number "n" is determined by the formula:

$n >= (Vnoise + |Vx1-Vx2|) / V_T$

where:

n is the number of serially connected polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuit located between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,

Vx2 is the magnitude of the second power supply voltage source, and
V_T is the threshold voltage of each of the polycrystalline silicon diodes.

40. (Previously Presented) The integrated circuit of claim 39, wherein the first and second regions of each diode are formed on a region of shallow trench isolation that formed within the substrate.

41. (Previously Presented) The integrated circuit of claim 40, further comprising an insulating layer disposed between each region of shallow trench isolation and the substrate.

42. (Previously Presented) The integrated circuit of claim 39, wherein each diode further comprises an oxide layer formed over a portion of the first and second regions at the junction.

43. (Previously Presented) The integrated circuit of claim 39, wherein the first electrode of each diode is a cathode and the second electrode of each diode is an anode.

44. (Previously Presented) The integrated circuit of claim 43, wherein the impurity of the first type is an N-type impurity having a density of approximately 10^{15} atoms/cm^3 to approximately 10^{21} atoms/cm^3.

45. (Previously Presented) The integrated circuit of claim 43, wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^3 to approximately 10^{21} atoms/cm^3.

46. (Previously Presented) The integrated circuit of claim 43, wherein each of the polycrystalline diodes has a thickness of from approximately 1000Å to approximately 3000Å.

47. (Previously Presented) The integrated circuit of claim 43, wherein each diode has a thickness of from approximately 0.5 μm to approximately 100 μm .

48. (Cancelled)